REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

Claims 25-34 are pending for examination in this application. Claims 25, 27, 29, 33 and 34 are amended to better clarify the extraction of current through the current sense emitter separate from the main emitter without the introduction of any new matter.

The outstanding Action presents an improper request for formal drawings already submitted in the Office Action Summary Sheet that misstates the pending claims as 23-34 instead of 25-34, a rejection of Claims 25-33 under 35 U.S.C. § 103(a) as being unpatentable over Yanagisawa et al (U.S. Patent No. 5,874,750, Yanagisawa) in view of Takeda et al (1998 International Symposium article, Takeda) and a rejection of Claim 34 under 35 U.S.C. § 103(a) as being unpatentable over Yanagisawa in view of Takeda in further view of Horiguchi et al (U.S. Patent No. 5,910,675).

Initially, it is again noted that the drawings filed on December 19, 2002 have not been properly acknowledged as the Office Action Summary Sheet simply indicates approval of the proposed correction filed on July 19, 2002, without acknowledging receipt of the Formal Drawings filed on December 19, 2002, that included the approved corrections. Copies of these 18 sheets of Formal Drawings and a copy of the date-stamped filing receipt indicating PTO receipt of these 18 sheets of Formal Drawings were included with the response filed on June 30, 2003, along with a request for proper acknowledgement of the filing of these 18 sheets of Formal Drawings. This request for a proper acknowledgement of the filing of these 18 sheets of Formal Drawings was repeated in the Amendment filed December 24, 2003, and the Supplemental Amendment filed March 23, 2004. This acknowledgement is now requested for the fourth time.

Turning to the rejection of Claims 25-33, the outstanding Action mistakenly reasserts that Yanagisawa teaches an injection enhanced gate transistor (IEGT) having a main emitter and a current sense emitter. However, even a cursory reading of Yanagisawa reveals that the teachings thereof relate to an insulated gate bipolar transistor (IGBT), not an IEGT. The IGBT of Yanagisawa has an emitter electrode plate 16 and a collector electrode plate to form a pressure-contact type IGBT which comprises a single-emitter structure and an emitter sensing terminal ES directly connected with the single emitter for monitoring the emitter voltage (which is a potential difference between the emitter on the IGBT chip and the ground of the gate circuit), so that the emitter sensing terminal is not influenced by inductance between the signal emitter and the emitter sensing terminal. There is no question that the IGBT of Yanagisawa has a single main emitter and no separate current sense emitter unlike the IEGT of independent Claims 25, 27, 29, 31, and 33.

A symbol of an IGBT is shown in the broken line circle in FIG. 8 of Yanagisawa that clearly shows the emitter to which the emitter voltage sensing terminal ES is connected. On the other hand, the IEGT has two separate emitters, and a symbol thereof is shown in FIG. 24 of the present application in which a main emitter of the IEGT chip 42a is connected to the emitter press-contacting electrode plate 47 via the inductance53a (see the specification at page 42, lines 14-16, for example), and a sense-side emitter of the IEGT chip 42a is connected to the gate of a transistor Tr and one terminal of a resistor Rs (see the specification at page 42, lines 23-25, for example). It is commonly known in the art that the main emitter and sense emitter are separately and isolatedly formed in an IEGT chip and the symbol thereof is shown in FIG. 24 (see page 42, lines 7-9 of the specification, for example).

As disclosed in column 1, lines 62-65 of Yanagisawa, an emitter voltage sensing terminal is needed to sense (monitor) voltage of an emitter electrode of the IGBT. This means that the emitter voltage sensing terminal is to be connected directly to the emitter

electrode which is connected to the emitter region of the IGBT. As shown in FIG. 7 of Yanagisawa, the emitter electrode 12 is connected to the emitter region 38 and the emitter sensing electrode 12a is connected to the emitter voltage sensing terminal ES. The emitter electrode 12 and the emitter voltage sensing terminal ES are shown part in FIG. 7, however, these elements are commonly formed by a single emitter electrode 37 as shown in FIG. 6 (see column 5, lines 29-32 of Yanagisawa).

In other words, the emitter voltage sensing terminal of the IGBT taught by Yanagisawa is to be connected directly to the emitter electrode so as to sense the emitter voltage. If the sensing terminal is connected to a portion separated from the emitter electrode, the correct emitter voltage cannot be detected.

On the contrary, the IEGT of Claims 25-33 must have the current sense emitter in addition to the main emitter.

Thus, the emitter configuration of the IGBT taught by Yanagisawa is utterly different from that of the IEGT of the present application.

As further noted in the December 24 Amendment, Takeda shows no more than an IEGT with a trench gate that has a multi-emitter structure for an over current limiting circuit.

Therefore, it is again clear that Yanagisawa shows no more than a pressure-contact type IEGT having an emitter voltage sensing terminal connected to a main emitter and that Takeda shows no more than an IEGT having a double-emitter structure and does not show a pressure-contact type IEGT having a current sense emitter. Accordingly, even if the structure taught by Yanagisawa were to be modified by or combined with that shown by Takeda, the pressure-contact type IEGT having a current sense emitter separate from the main emitter as recited in the amended independent claims is not the result and no *prima facie* case of obviousness has been established as to the subject mater of Claims 25-33.

Turning to the rejection of Claim 34 under 35 U.S.C. § 103(a) as being unpatentable over Yanagisawa in view of Takeda in further view of Horiguchi, it is note that Horiguchi cures none of the deficiencies noted above as to Yanagisawa and Takeda. In this regard, Horiguchi only teaches a transistor 5 and a resistor 7 connected to the gate of the transistor 5, see FIG. 1. However, the gate of the transistor 5 is not connected to receive a current extracted from a current sense emitter unlike the present invention recited in Claim 34. Therefore, the subject matter recited in Claim 34 is not obvious over Yanagisawa in view of Takeda and further in view of Horiguchi.

In view of the above comments and the further comments set forth in the December 24 Amendment, it is respectfully submitted that no issues remain outstanding relative to the present application, which is, therefore, clearly in condition for formal allowance. Accordingly, an action to that effect is respectfully requested.

Respectfully submitted,

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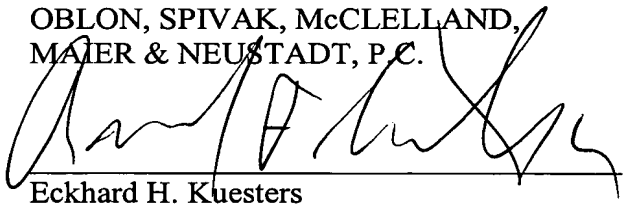

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